

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
SO_DDRIII DIMMA1&SO_DDRIII DIMMB1	7,8
PPT-PCI/E/DMI/CLK/USB20/USB30	9
PPT-SATA/HOST/GPIO/VGA/CCMOS	10
PPT-SMB/LPC/AUDIO/RTC/SPI	11
PPT-POWER,GND/NVRAM /CP STRAPS	12,13,14
PCIE Slot	15
PCI Slot	16
LAN - RTL8111E/8105	17
AUDIO 887	18
VGA/HDMI	19,20
USB2.0/3.0 Connector/SATA Connector	21,22,23
SIO-Fintek F71868AD	24
FAN	25
ATX F_Panel/EMI/TPM	26
ACPI Controller UPI	27
VRM12 - UT501colay UT1654P	28
UP6282 3-Phase+MOS CPU	29
UP6282 1-Phase+MOS GPU	30
UP1513 - VTT POWER	31
OP+MOS - SA POWER	32
UP1513 - DDR POWER	33
PCH POWER	34
ME Power - UP1712	35
XDP / Manual Parts	36
EMI CAP	37

MS-7808

ATX
Ver:0A

H/W: Frankyang
PM: Feifei

Intel -MahoBay plamform B75

CPU:
IVY bridge LGA1155

Onboard Chip:
Audio Codec: 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 128 MB

System Chipset:
Panther Point B75

Main Memory:
DDRIII (1066/1333/1600MHz)
* 2 (Dual Channel)

ACPI:
UPI

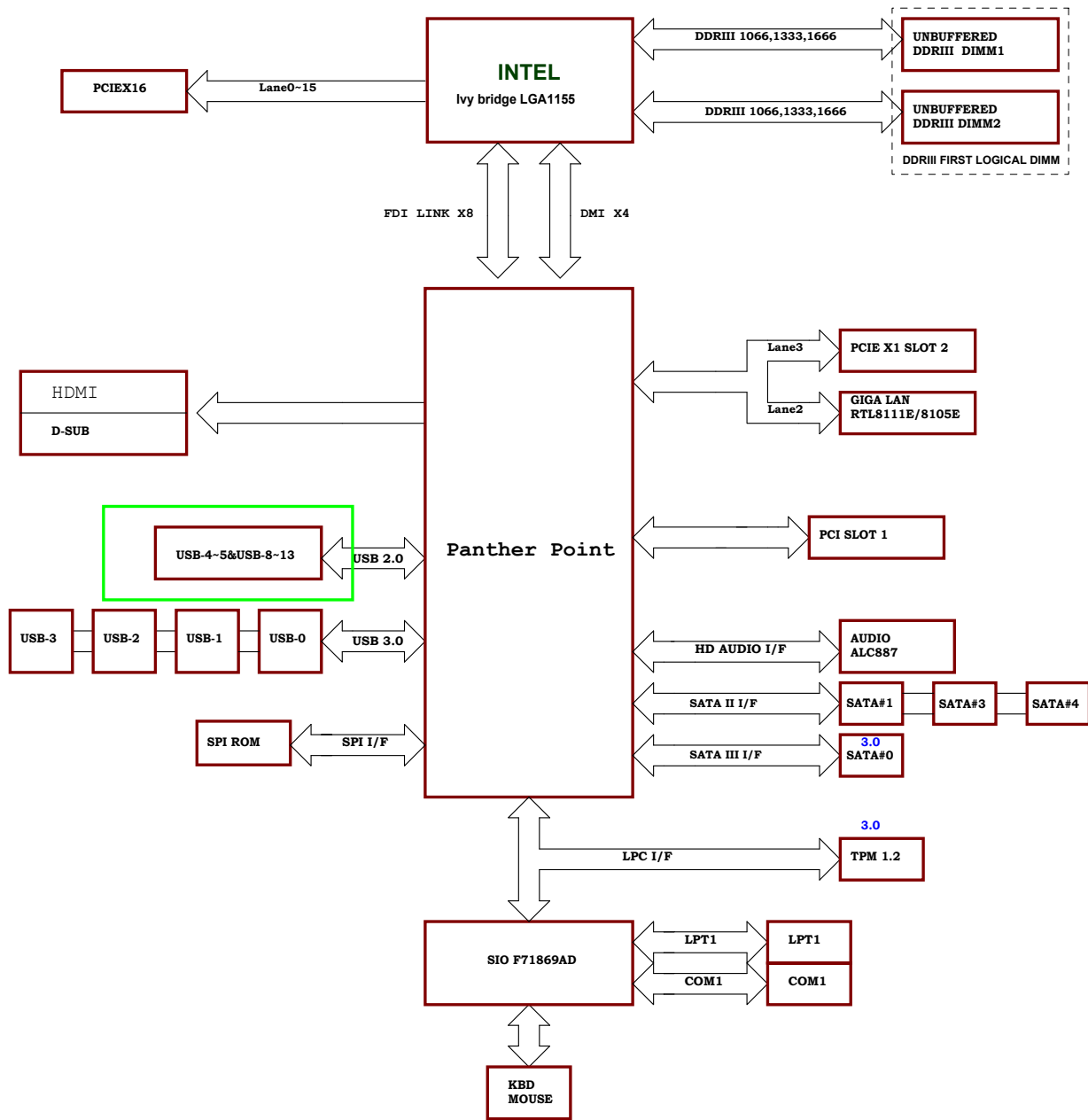
Expansion Slots:
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1
PCI Slot * 1

PWM:
VRD12 -UT501 3+1 Phase

Other:
SATA3.0 x1+SATA2.0 x3 (PCH)
USB2.0 *8
REAL USB3.0 *2
FRONT USB3.0 *2

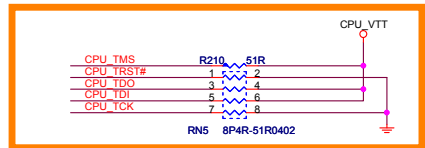


MS-7758 Block Diagram

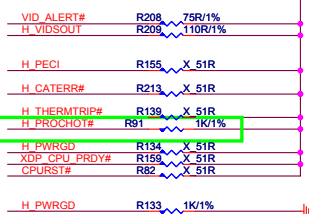


Slot Sequence:

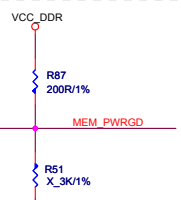
- PCIEX16
- PCIEX1
- PCI SLOT



TCK/TDI/TMS TERMINATION NEAR CPU CPU_VTT

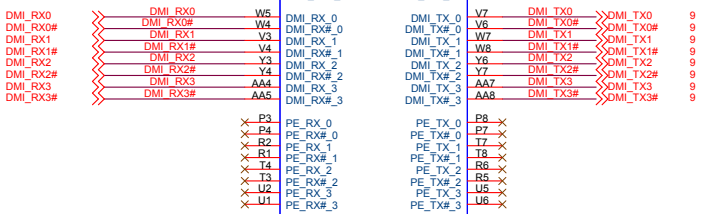
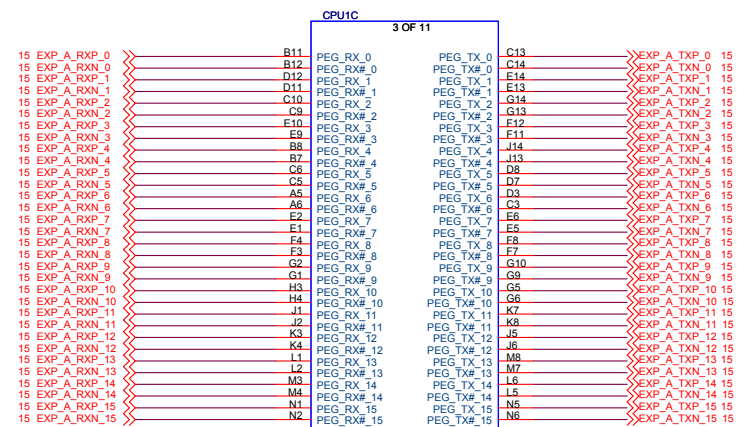
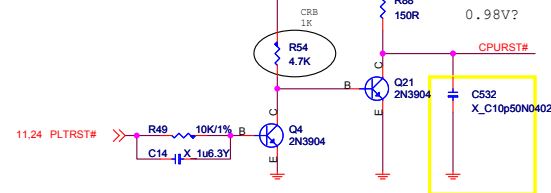


Power On
Hardware default = high



1. Set GPIO2 Data = 1
 2. Set GPIO2 port as output by open-drain mode
 3. Porting GPIO2 Data = 0 before system into deep_s3
 4. Waiting CPU_PWRGD from low to high and setting GPIO2_Data = 1 when resume from deep_s3
- GPIO2 always keep high except for deep_s3

CPU_RESET#
CPURST# rise/fall time <6ns



CPU1I
9 OF 11

A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A25	VSS_003	VSS_093	AM30
A26	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM6
AA35	VSS_008	VSS_098	AW10
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AW16
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AW6
AC1	VSS_014	VSS_104	AY11
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AY18
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD8	VSS_021	VSS_111	AN32
AE3	VSS_022	VSS_112	B13
AE33	VSS_023	VSS_113	AN33
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	B23
AE1	VSS_026	VSS_116	AN6
AF34	VSS_027	VSS_117	AN6
AF36	VSS_028	VSS_118	AN7
AF37	VSS_029	VSS_119	B36
AF40	VSS_030	VSS_120	AN8
AF5	VSS_031	VSS_121	B38
AF6	VSS_032	VSS_122	AP1
AG36	VSS_033	VSS_123	AP11
AH2	VSS_034	VSS_124	C12
AH3	VSS_035	VSS_125	AP17
AH33	VSS_036	VSS_126	AP22
AH36	VSS_037	VSS_127	AP25
AH37	VSS_038	VSS_128	AP27
AH38	VSS_039	VSS_129	AP30
AH38	VSS_040	VSS_130	AP36
AH38	VSS_041	VSS_131	AP37
AH40	VSS_042	VSS_132	C74
AH5	VSS_043	VSS_133	AP40
AH6	VSS_044	VSS_134	AP5
A112	VSS_045	VSS_135	AR11
A115	VSS_046	VSS_136	AR14
A118	VSS_047	VSS_137	AR17
A121	VSS_048	VSS_138	AR18
A125	VSS_049	VSS_139	AR27
A127	VSS_050	VSS_140	AR30
A136	VSS_051	VSS_141	AR36
A15	VSS_052	VSS_142	D4
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	F2
AK8	VSS_072	VSS_162	F20
AK9	VSS_073	VSS_163	F23
AL11	VSS_074	VSS_164	F26
AL14	VSS_075	VSS_165	F28
AL17	VSS_076	VSS_166	F35
AL19	VSS_077	VSS_167	F37
AL24	VSS_078	VSS_168	F39
AL27	VSS_079	VSS_169	F5
AL30	VSS_080	VSS_170	F6
AL36	VSS_081	VSS_171	F9
AL5	VSS_082	VSS_172	G11
AM1	VSS_083	VSS_173	G12
AM11	VSS_084	VSS_174	G17
AM14	VSS_085	VSS_175	G20
AM17	VSS_086	VSS_176	G23
AM2	VSS_087	VSS_177	G26
AM21	VSS_088	VSS_178	G29
AM23	VSS_089	VSS_179	G34
AM25	VSS_090	VSS_180	G7

LGA1155

CPU1J
10 OF 11

AV11	VSS_181	VSS_281	H37
AV17	VSS_182	VSS_282	H39
AV3	VSS_183	VSS_283	H5
AV35	VSS_184	VSS_284	H6
AV38	VSS_185	VSS_285	H9
AV6	VSS_186	VSS_286	J11
AW10	VSS_187	VSS_287	J17
AW11	VSS_188	VSS_288	J20
AW14	VSS_189	VSS_289	J23
AW16	VSS_190	VSS_290	J26
AW36	VSS_191	VSS_291	J29
AW6	VSS_192	VSS_292	J32
AY11	VSS_193	VSS_293	K1
AY14	VSS_194	VSS_294	K12
AY18	VSS_195	VSS_295	K13
AY22	VSS_196	VSS_296	K14
AY35	VSS_197	VSS_297	K17
AY4	VSS_198	VSS_298	K2
AY6	VSS_199	VSS_299	K20
AY8	VSS_200	VSS_300	K23
B10	VSS_201	VSS_301	K26
B13	VSS_202	VSS_302	K29
B14	VSS_203	VSS_303	K33
B17	VSS_204	VSS_304	K35
B23	VSS_205	VSS_305	K37
B26	VSS_206	VSS_306	K39
B29	VSS_207	VSS_307	K5
B32	VSS_208	VSS_308	K6
B36	VSS_209	VSS_309	L10
B6	VSS_210	VSS_310	L17
C12	VSS_211	VSS_311	L20
C17	VSS_212	VSS_312	L23
C20	VSS_213	VSS_313	L26
C23	VSS_214	VSS_314	L29
C26	VSS_215	VSS_315	L8
C29	VSS_216	VSS_316	M1
C32	VSS_217	VSS_317	M17
C35	VSS_218	VSS_318	M2
C74	VSS_219	VSS_319	M20
C8	VSS_220	VSS_320	M23
D17	VSS_221	VSS_321	M28
D2	VSS_222	VSS_322	M29
D20	VSS_223	VSS_323	M33
D23	VSS_224	VSS_324	M35
D26	VSS_225	VSS_325	M37
D29	VSS_226	VSS_326	M39
D32	VSS_227	VSS_327	M5
D37	VSS_228	VSS_328	M6
D39	VSS_229	VSS_329	M9
D4	VSS_230	VSS_330	N8
D5	VSS_231	VSS_331	P1
D9	VSS_232	VSS_332	P2
E11	VSS_233	VSS_333	P36
E12	VSS_234	VSS_334	P38
E17	VSS_235	VSS_335	P40
E20	VSS_236	VSS_336	P5
E23	VSS_237	VSS_337	P6
E26	VSS_238	VSS_338	R33
E29	VSS_239	VSS_339	R35
E36	VSS_240	VSS_340	R37
E7	VSS_241	VSS_341	R39
E8	VSS_242	VSS_342	R8
F1	VSS_243	VSS_343	T1
F10	VSS_244	VSS_344	T5
F13	VSS_245	VSS_345	T6
F14	VSS_246	VSS_346	U8
F17	VSS_247	VSS_347	V1
F2	VSS_248	VSS_348	V2
F20	VSS_249	VSS_349	V33
F23	VSS_250	VSS_350	V34
F26	VSS_251	VSS_351	V35
F28	VSS_252	VSS_352	V36
F35	VSS_253	VSS_353	V37
F37	VSS_254	VSS_354	V38
F39	VSS_255	VSS_355	V39
F5	VSS_256	VSS_356	V40
F6	VSS_257	VSS_357	V5
F9	VSS_258	VSS_358	V6
G11	VSS_259	VSS_359	V5
G12	VSS_260	VSS_360	Y8
G17	VSS_261		
G20	VSS_262		
G23	VSS_263		
G26	VSS_264		
G29	VSS_265		
G34	VSS_266		
G7	VSS_267		
H1	VSS_268		
H17	VSS_269		
H2	VSS_270		
H20	VSS_271		
H23	VSS_272		
H26	VSS_273		
H29	VSS_274		
H33	VSS_275		
H35	VSS_276		
	VSS_277		
	VSS_278		
	VSS_279		
	VSS_280		

LGA1155

CPU1K
11 OF 11

×C40	RSVD_001	RSVD_036	L33
×D40	RSVD_002	RSVD_037	L34
×AB6	RSVD_003	RSVD_038	L9
×AB7	RSVD_004	RSVD_039	M34
×AD37	RSVD_005	RSVD_040	N33
×AE6	RSVD_006	RSVD_041	N34
×AF4	RSVD_007	RSVD_043	P35
×AG4	RSVD_008	RSVD_044	P36
×A111	RSVD_009	RSVD_045	P37
×A129	RSVD_010	RSVD_046	P38
×A130	RSVD_011	RSVD_047	P39
×A131	RSVD_012	RSVD_048	R40
×AN20	RSVD_013	RSVD_049	R41
×AP20	RSVD_014	RSVD_051	AD34
×AT11	RSVD_015	RSVD_052	AD35
×AU10	RSVD_016	RSVD_053	K31
×AV1	RSVD_017		
×AV34	RSVD_018		
×AW2	RSVD_019		
×AW34	RSVD_020		
×AX3	RSVD_021		
×B39	RSVD_022		
×C38	RSVD_023		
×C39	RSVD_024		
×D36	RSVD_025		
×H7	RSVD_026		
×H8	RSVD_027		
×J33	RSVD_028		
×J34	RSVD_029		
×J9	RSVD_030		
×K34	RSVD_031		
×K9	RSVD_032		
×L31	RSVD_033		
×L31	RSVD_034		
×L31	RSVD_035		

FC_AH1

FC_AH4

NCTF_01

NCTF_02

NCTF_03

NCTF_04

NCTF_05

NCTF_06

NCTF_07

NCTF_08

NCTF_09

NCTF_10

NCTF_11

NCTF_12

NCTF_13

NCTF_14

NCTF_15

NCTF_16

NCTF_17

NCTF_18

NCTF_19

NCTF_20

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NCTF_98

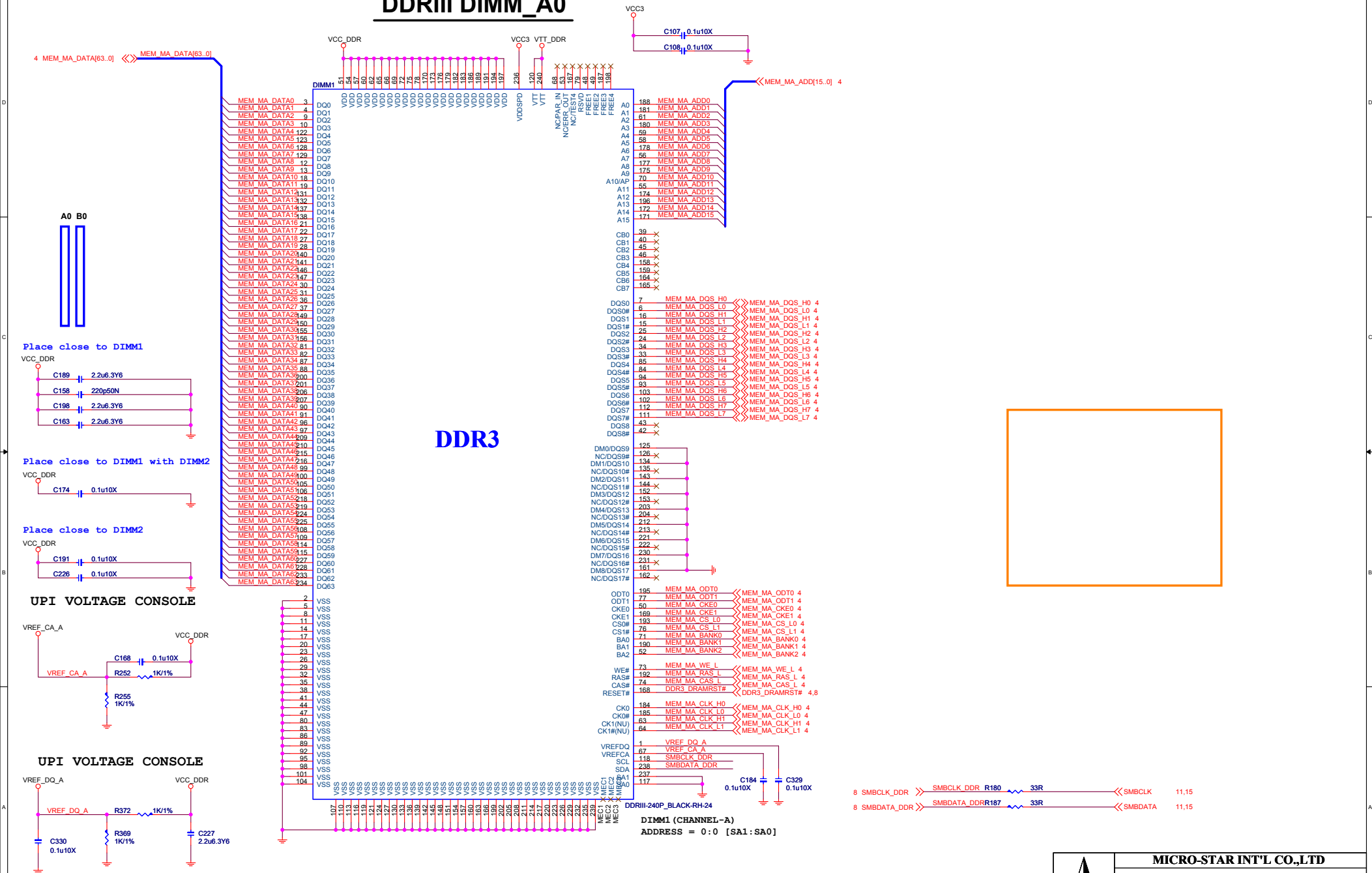
NCTF_99

NCTF_100

NCTF_101

NCTF_102

DDRIII DIMM_A0

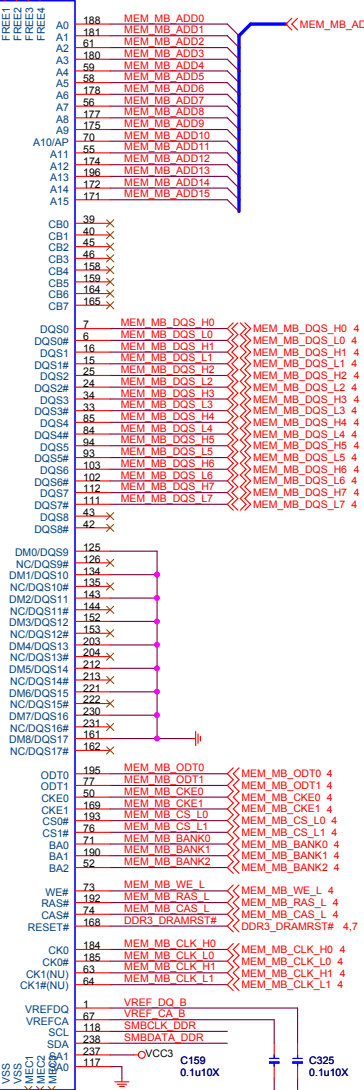


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MS-7808

Size Custom	Document Description DDR3 Chanel-A DIMM1/2	Rev 0A
Date: Friday, May 11, 2012	Sheet 7 of 41	

DDR3

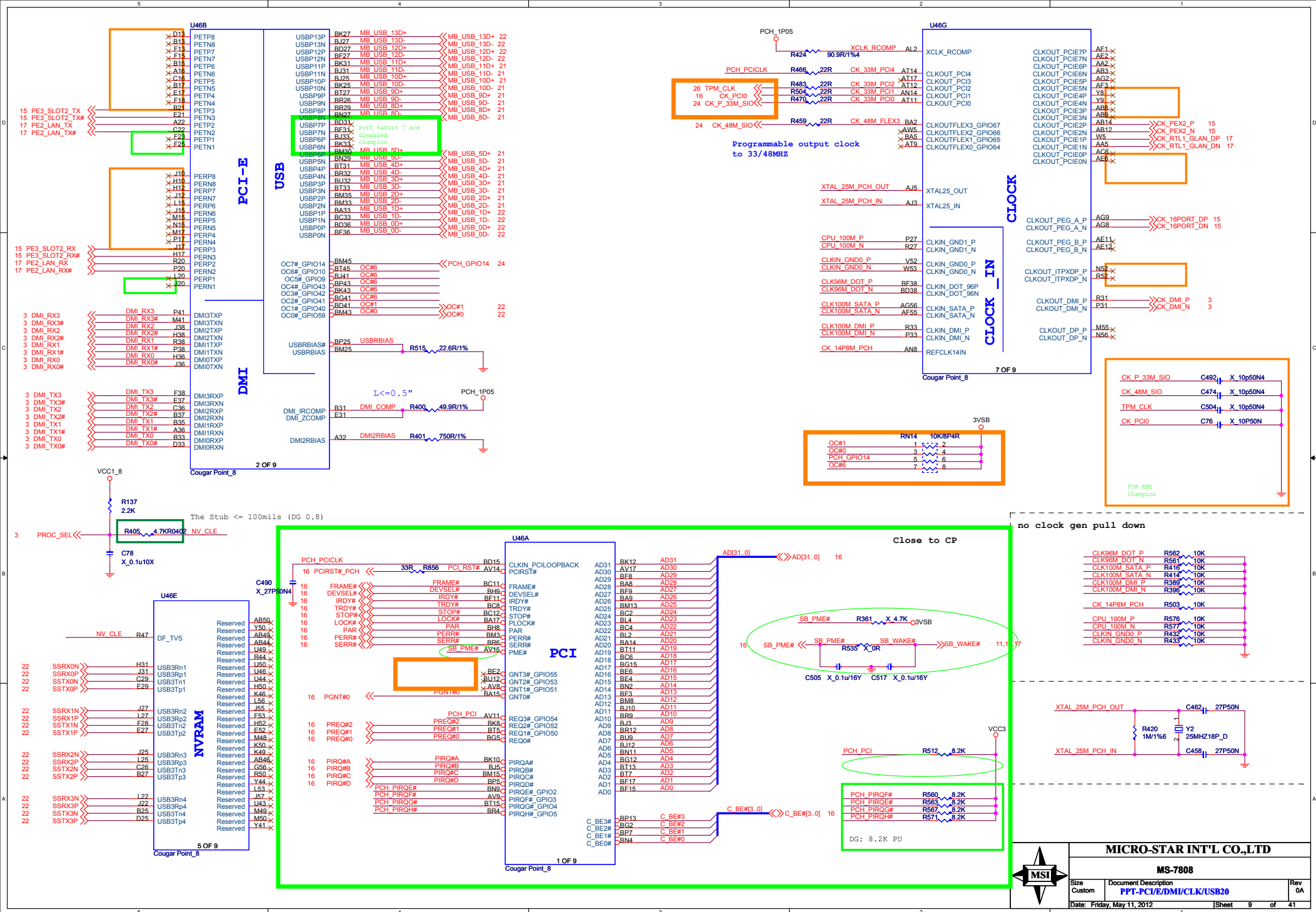


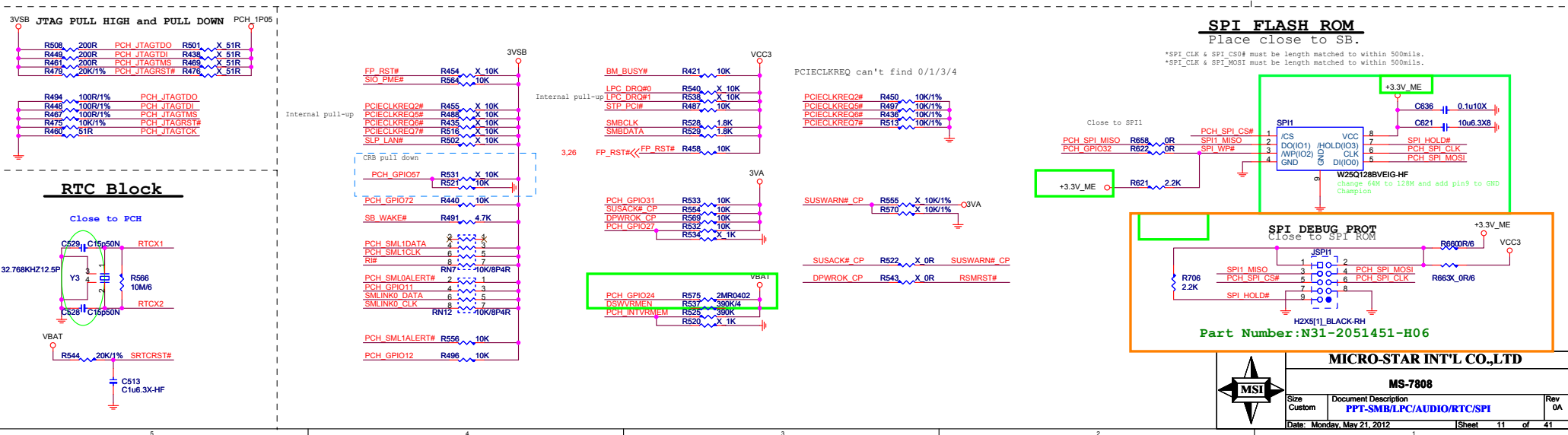
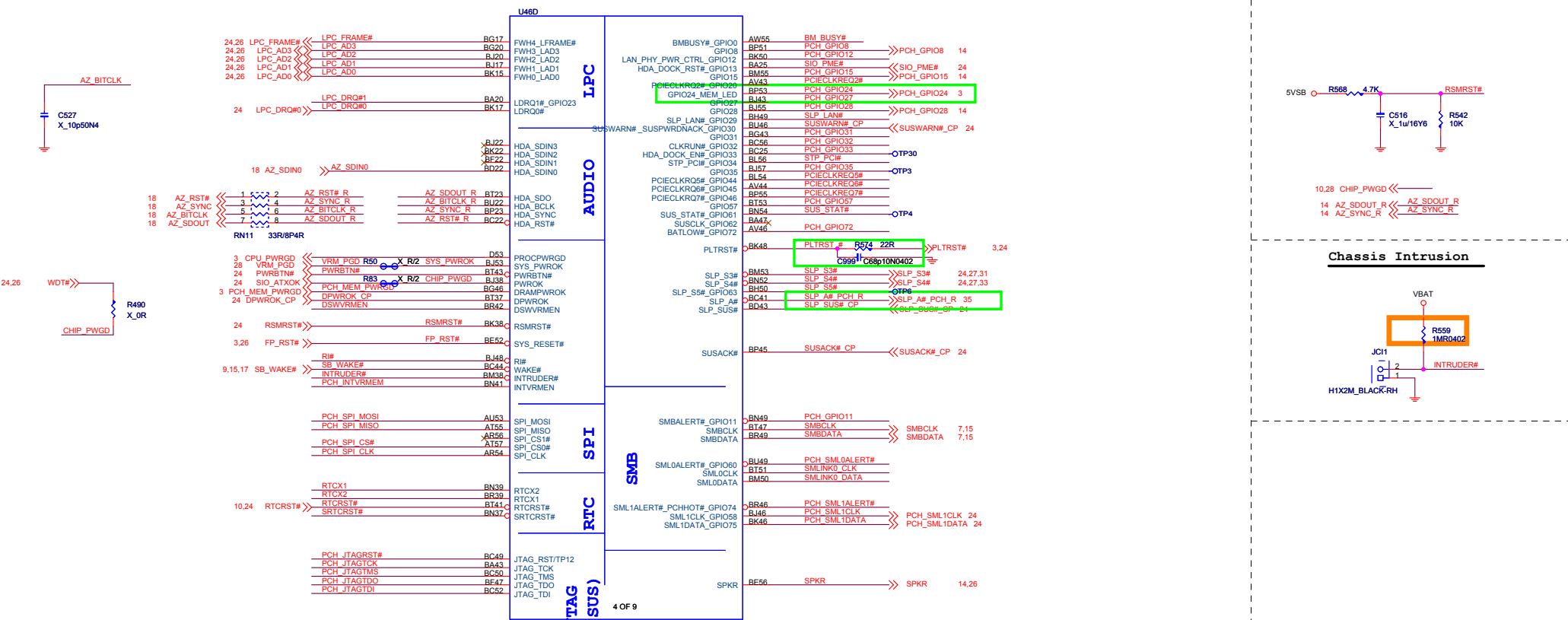
DIMM2 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]



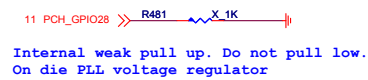
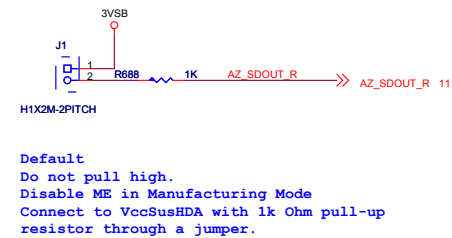
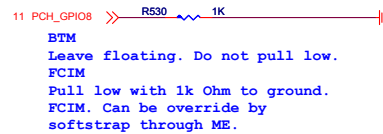
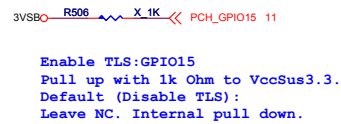
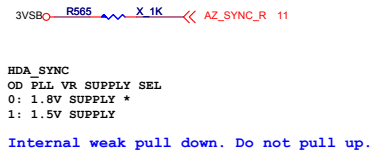
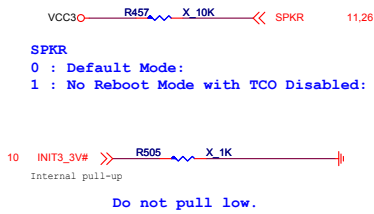
MS-7808

Size Custom	Document Description DDR3 Chanel-B DIMM3/4	Rev 0A
Date: Friday, May 11, 2012	Sheet 8 of 41	





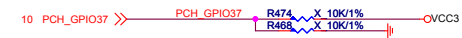
PCH Straps



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

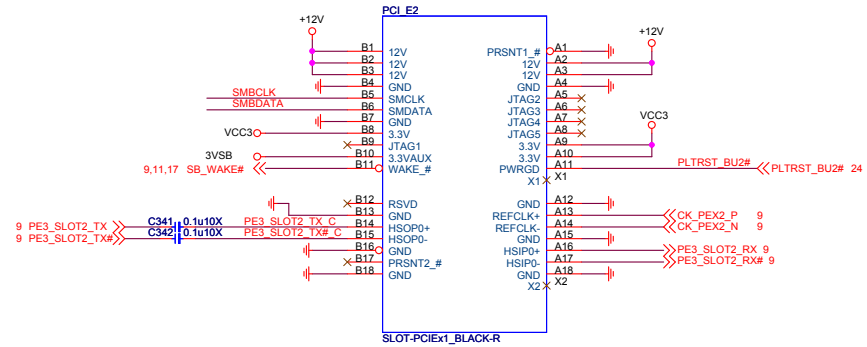
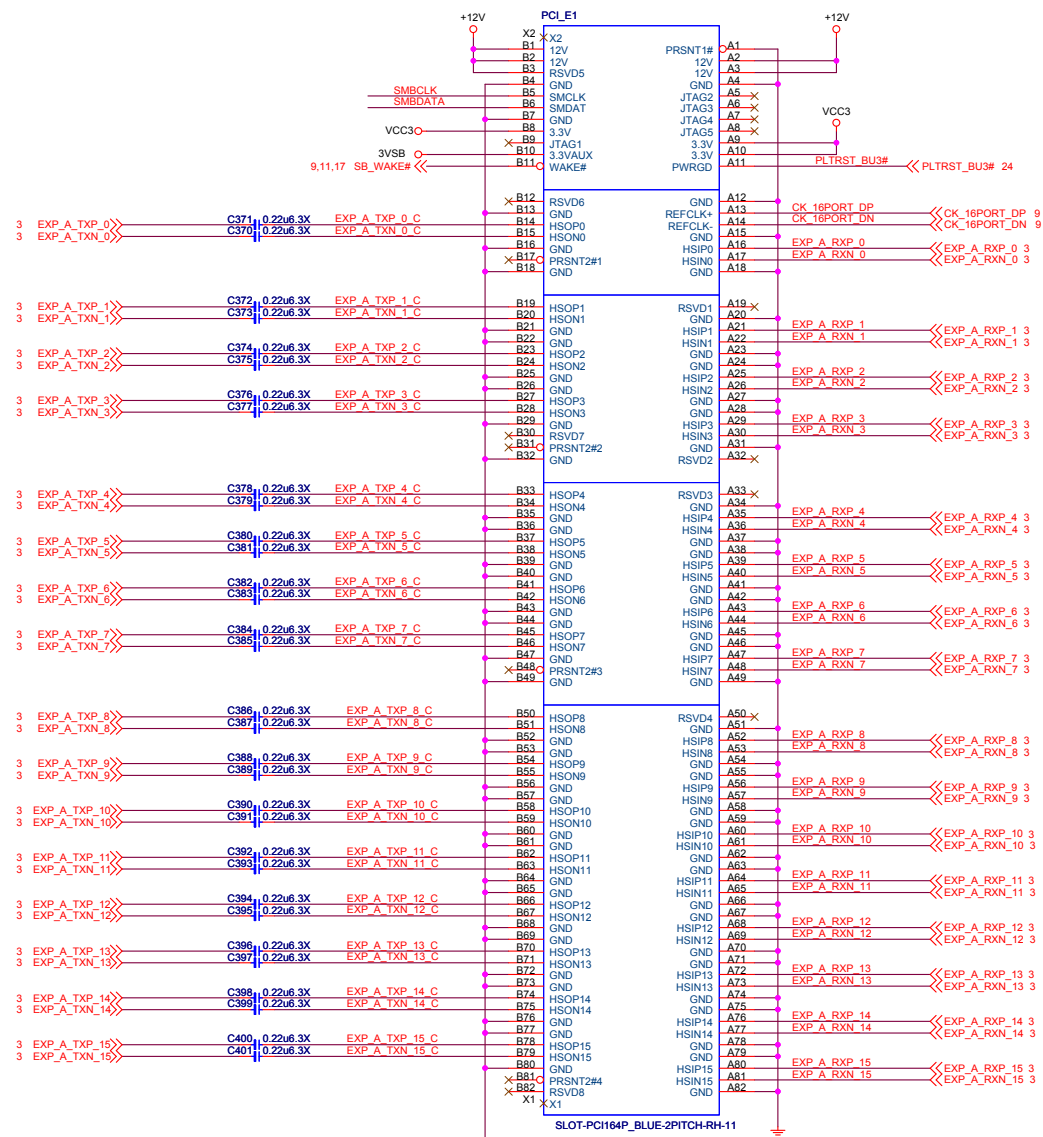


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

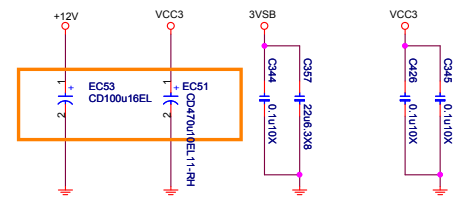
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

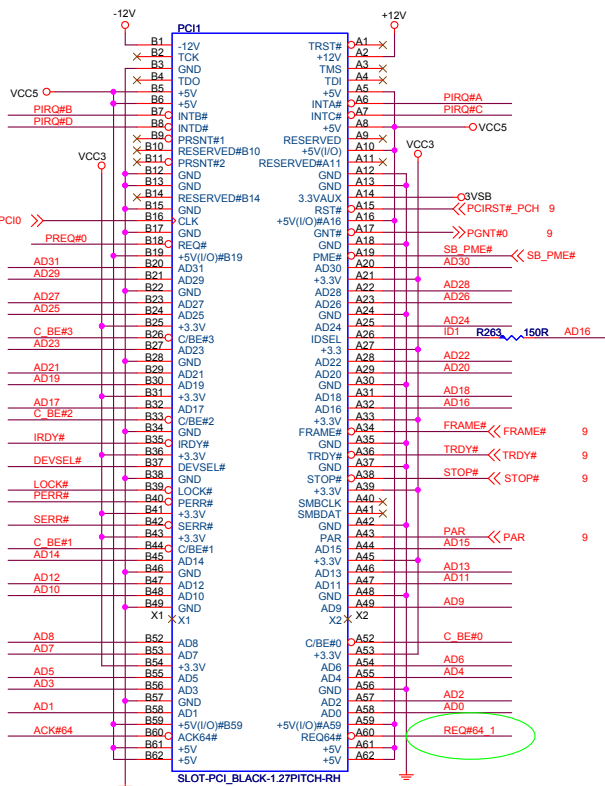
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

7,11 SMBCLK>> SMBCLK
7,11 SMBDATA>> SMBDATA



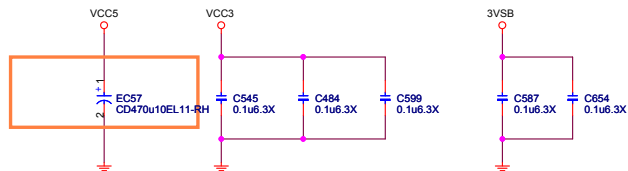
PCE slot	
+3.3Vaux	- 375mA
+3.3V	- 9A
+12V	- 6A



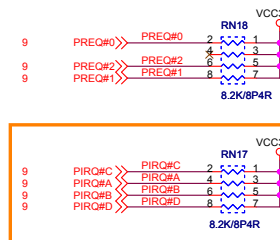
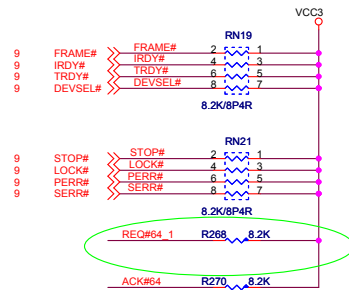


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] <<> AD[31..0] 9
 C_BE#[3..0] <<> C_BE#[3..0] 9



PCI PULL-UP / DOWN RESISTORS



Remove the pull up R of PGNT#0 Champion

PCI slot

+3.3Vaux	- 375mA
+3.3V	- 7.6A
+12V	- 0.5A



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MS-7808

Size	Document Description	Rev
Custom	PCI1 Slots	0A
Date: Friday, May 11, 2012	Sheet 16 of 41	

VCC3

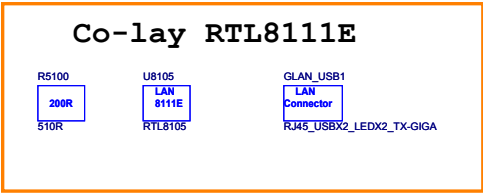
RL1 1K/4

RL2 15K/1%4

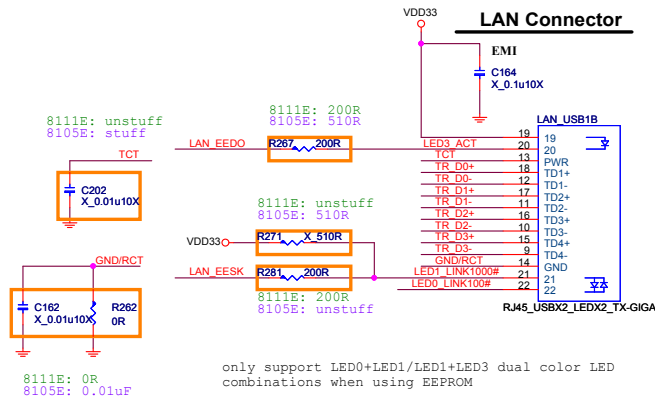
LAN ISO





ENSWREG:

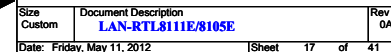
- 1: Enable switching regulator
- 0: Disable switching regulator



	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

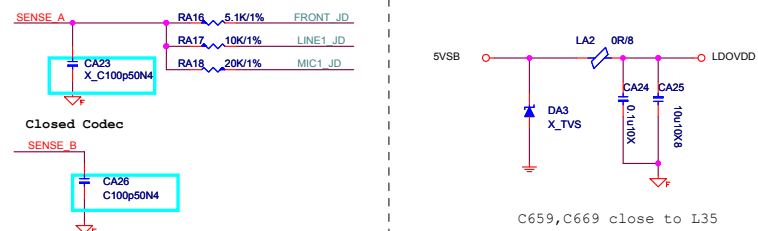
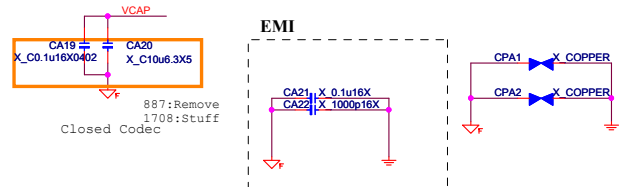
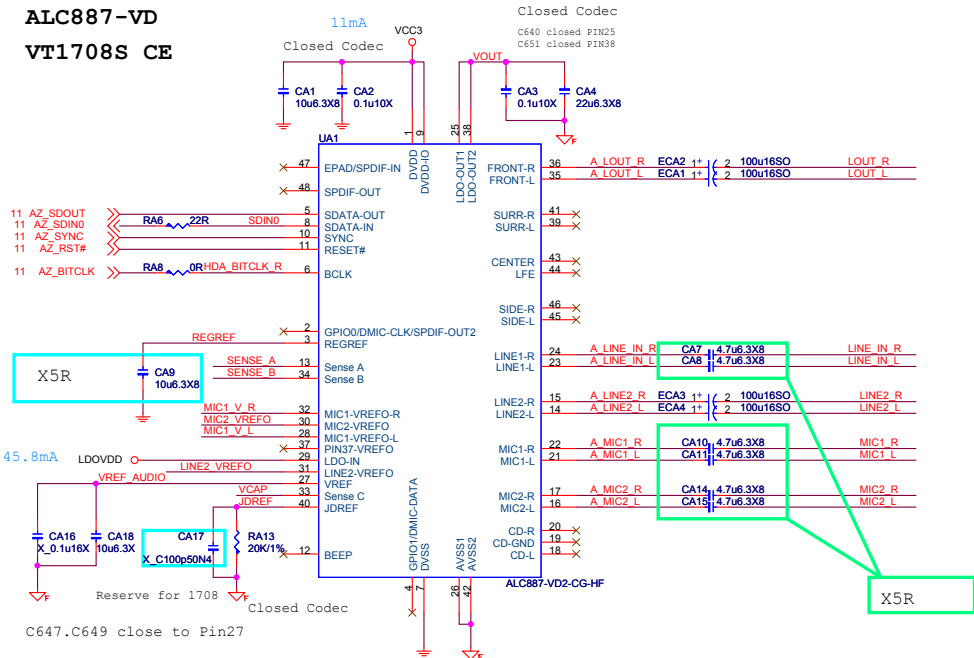


Giga-Lan		10/100-Lan	
<p>N58-22F0731</p> <p>Link Yellow Active Blinking 1000 Orange 100 Green 10 None</p>		<p>N58-22F0771</p> <p>Link Yellow Active Blinking 100 Green 10 None</p>	
<p>19 —————</p> <p>20 ———— 250R ————</p>	 <p>Yellow</p>	<p>19 —————</p> <p>20 ———— 250R ————</p>	 <p>Yellow</p>
<p>21 —————</p> <p>22 ———— 250R ————</p>	<p>Orange</p>  <p>Orange</p>	<p>21 —————</p> <p>22 ———— 250R ————</p>	 <p>Green</p>

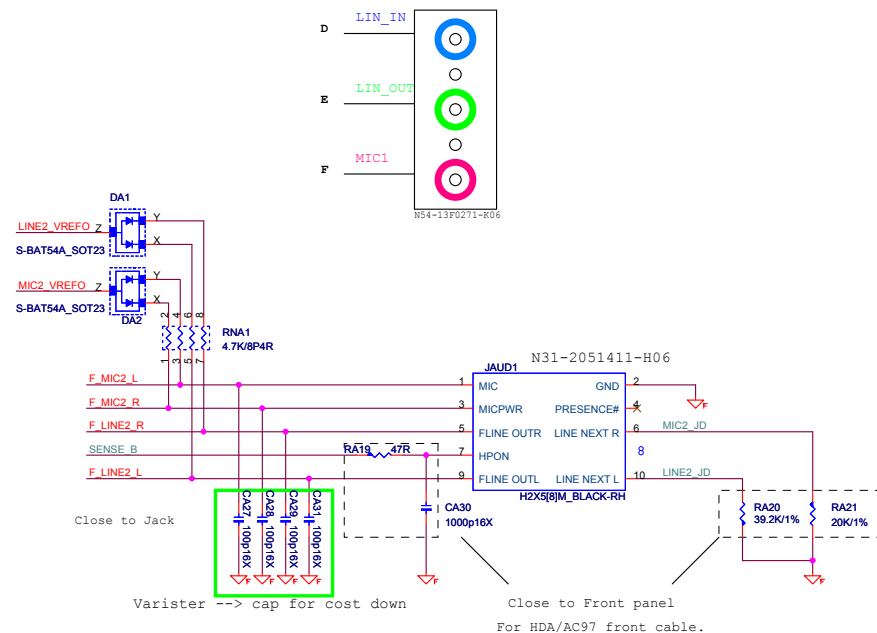
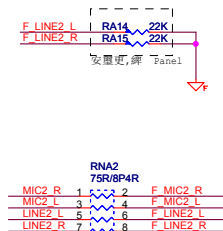
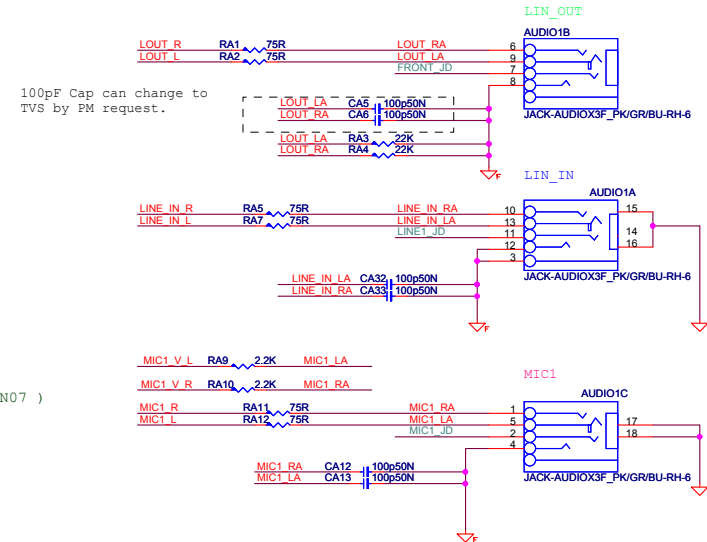


ALC887-VD

VT1708S CE



SPDIF OUT



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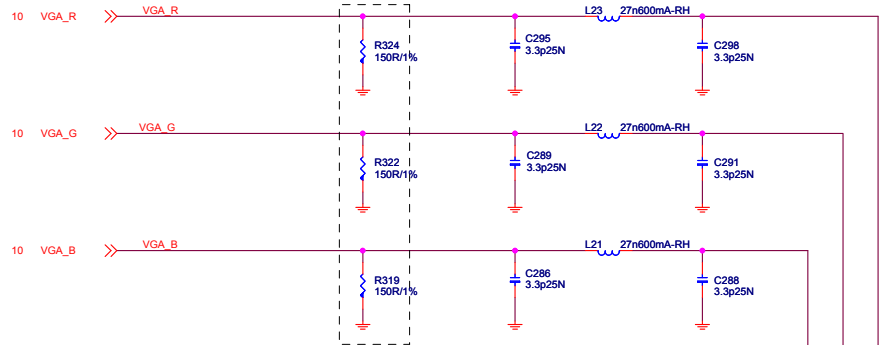
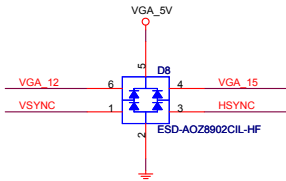
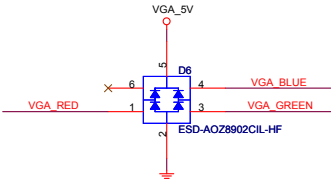
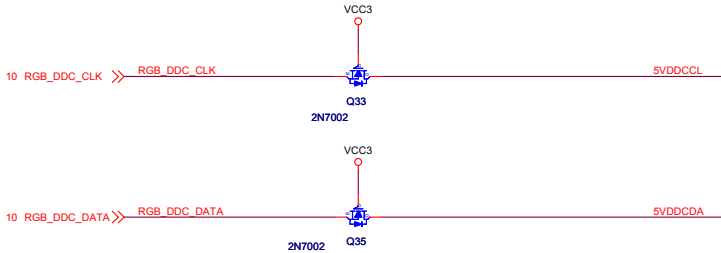
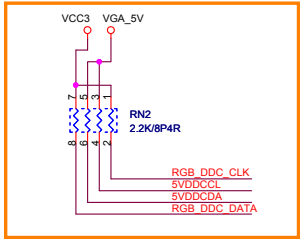
MS-7808

Size	Document Description	Rev
Custom	Audio Codec ALC887	0A
Date: Friday, May 11, 2012	Sheet 18 of 41	

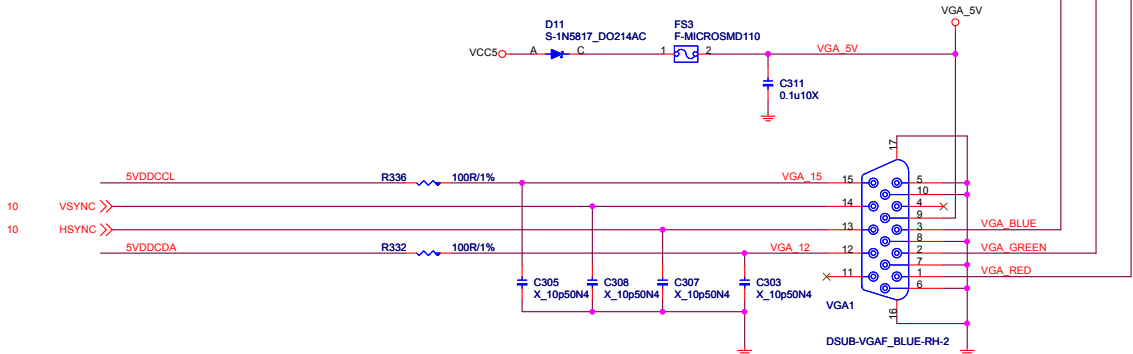
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

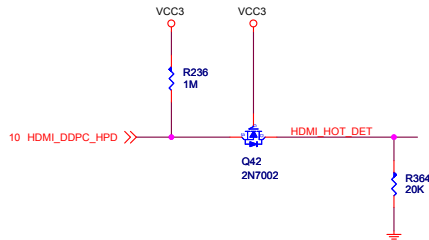
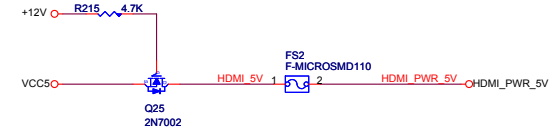
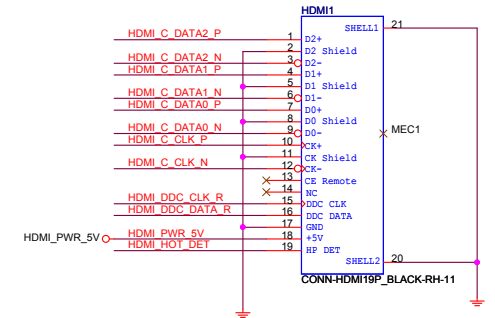
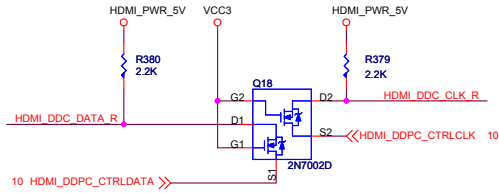
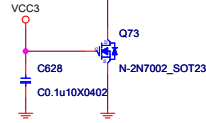
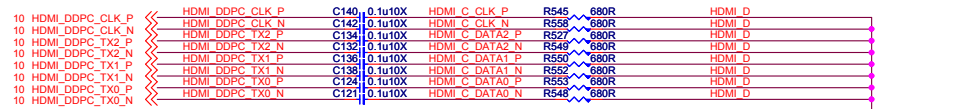
Level shift



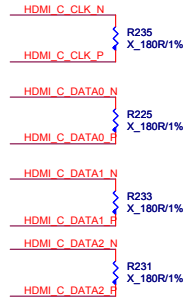
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



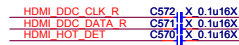
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



For EMI



EMI

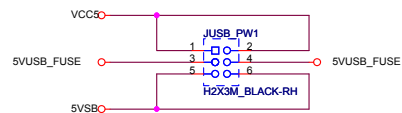


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MS-7808

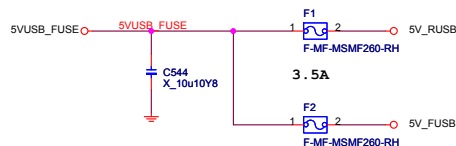
Size	Document Description	Rev
Custom	HDMI Connector	0A
Date: Friday, May 11, 2012	Sheet 20 of 41	

5V_RUSB Switch

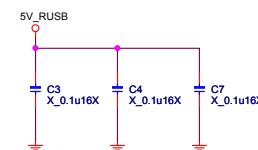
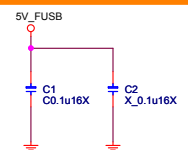


Default VCC5 (PIN1-3,2-4)

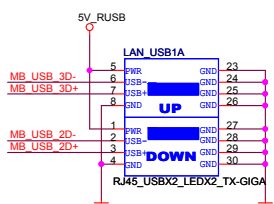
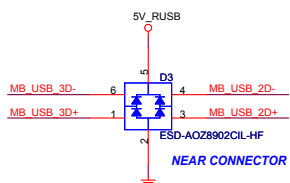
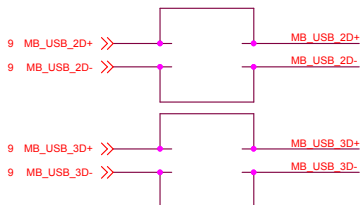
5V_RUSB must 120mm



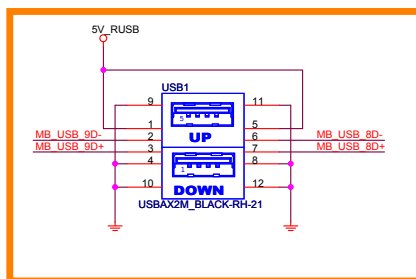
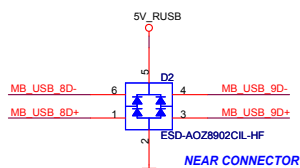
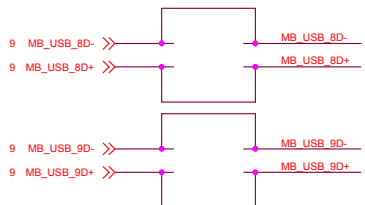
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	
3-5,4-6	EUP Enable	Not support
	EUP Disable	support



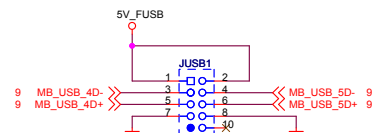
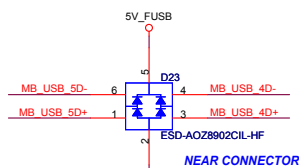
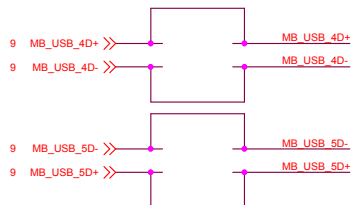
REAR USB PORT 8,9 (With LAN)



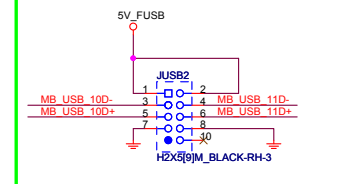
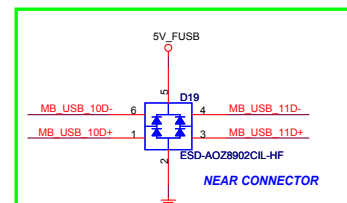
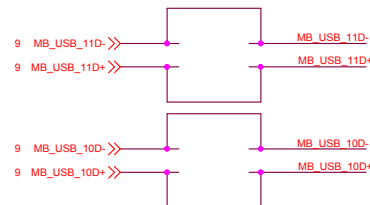
REAR USB PORT 8,9 (USB1)



FRONT USB PORT 0,1



FRONT USB PORT 8,9



Remove USB2.0 PORT 10,11
USB6&USB7
Champion



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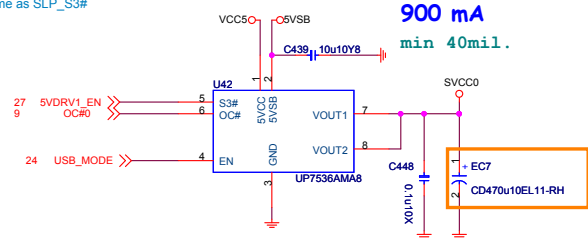
MS-7808

Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	0A
Date: Wednesday, May 23, 2012	Sheet 21 of 41	

FRONT USB30 PORT 0,1

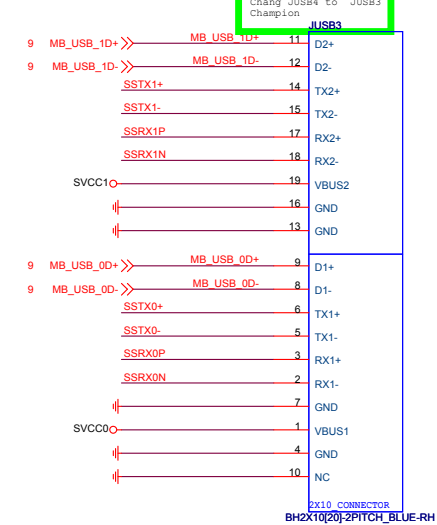
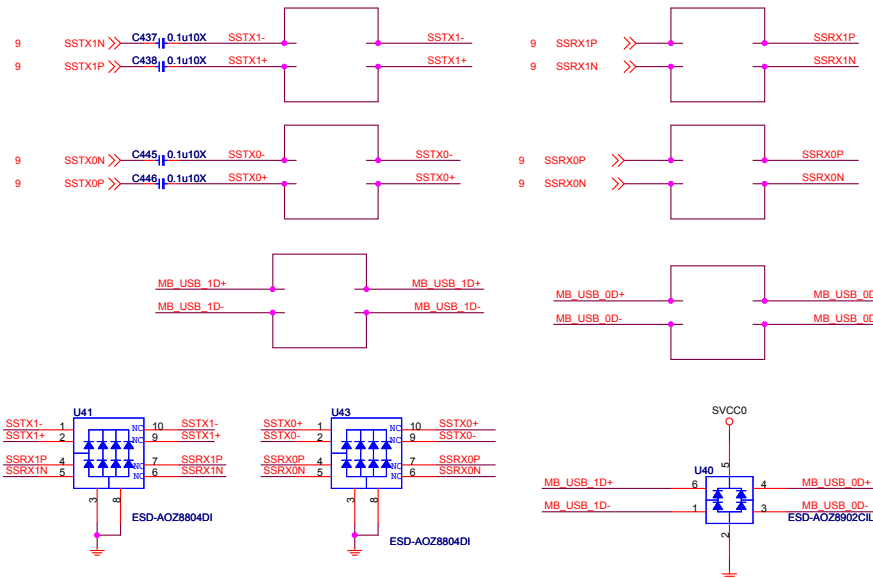
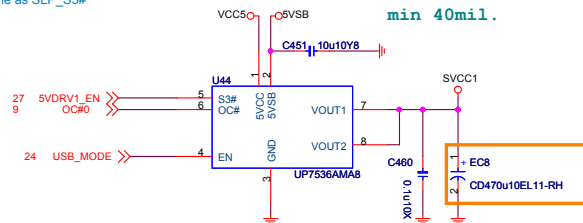
Same as SLP_S3#

900 mA
min 40mil.



Same as SLP_S3#

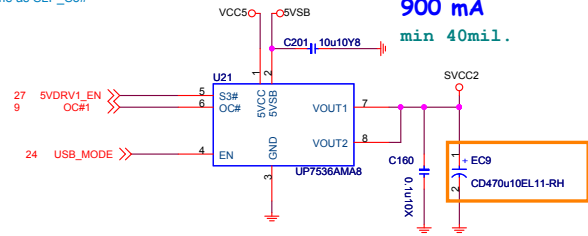
900 mA
min 40mil.



REAR USB30 PORT 2,3

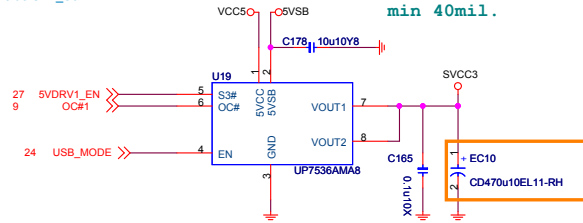
Same as SLP_S3#

900 mA
min 40mil.



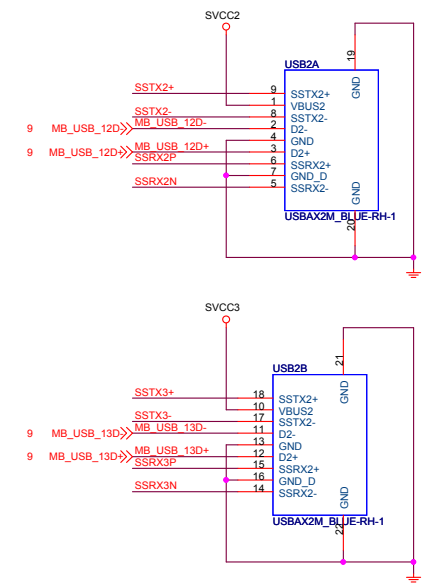
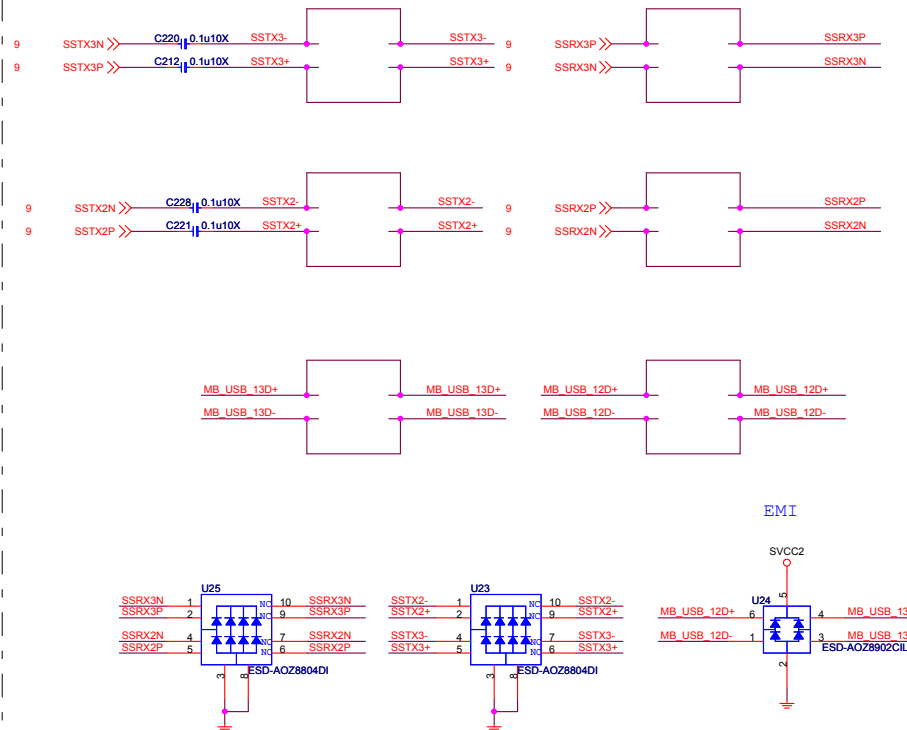
Same as SLP_S3#

900 mA
min 40mil.



USB_MODE
Hi by BIOS programming,
default h/w PD for avoid UP7536 Enable pin floating

USB MODE States					
MODE	G3	S4/S5	S0	S3	
EUP Disable	0	0	1	1	
EUP Enable	0	0	1	1	



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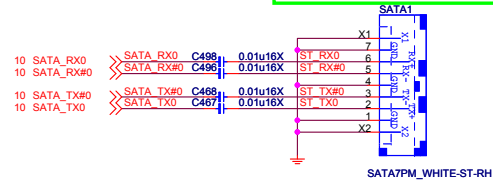
MS-7808

Size	Document Description	Rev
Custom	USB3.0 Connector	0A
Date: Monday, May 21, 2012	Sheet 22 of 41	

change SATA5s PORT0,1 to SATA PORT 0

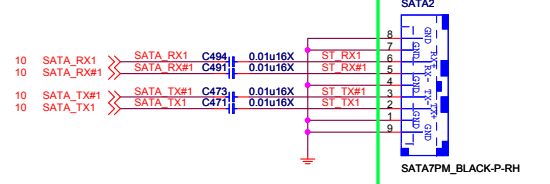
SATA 6G PORT 0

3.0 white

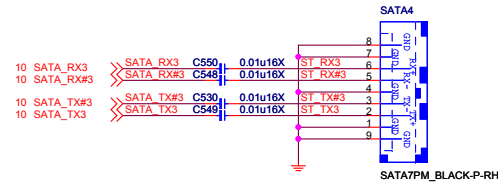
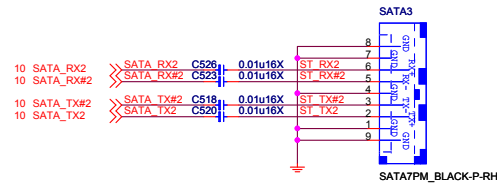


add - SATA 3G PORT 1
Champion

SATA 3G PORT 1



SATA 3G PORT 2,3



REMOVE SATA5\6 , Exchange name of sata1 with sata4



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MS-7808

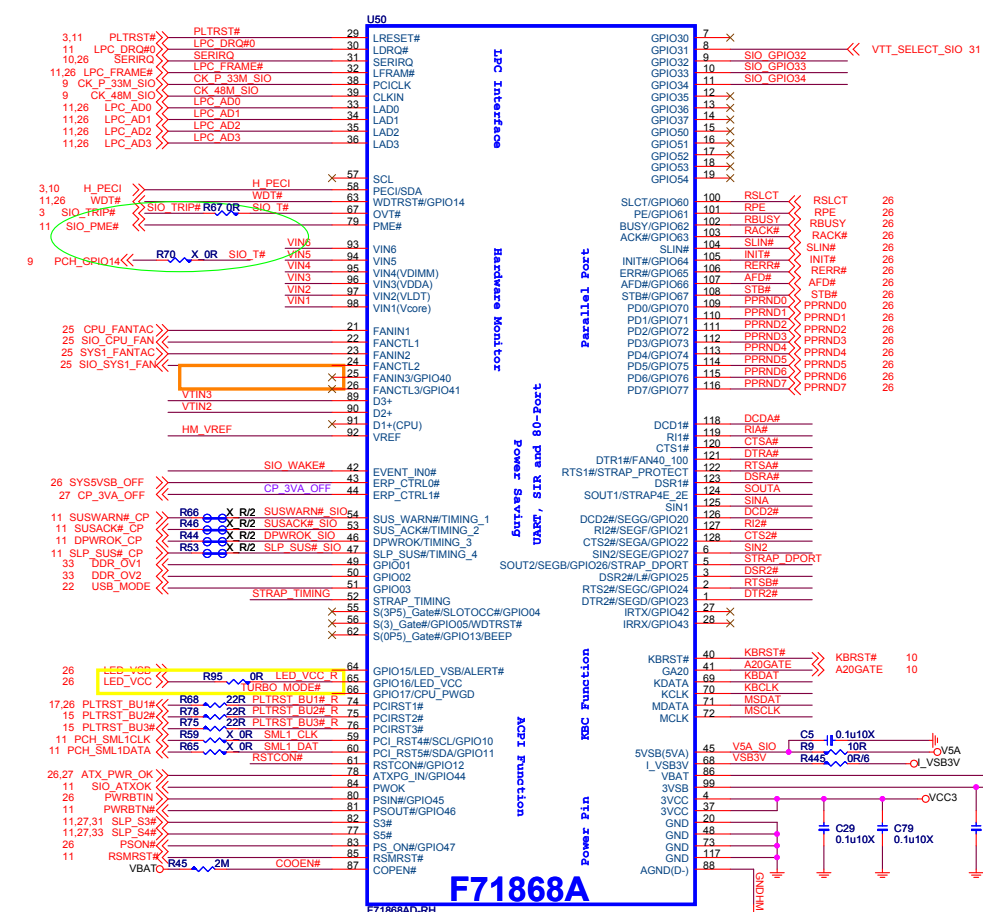
Size
Custom

Document Description
SATA Connector

Rev
0A

Date: Friday, May 11, 2012

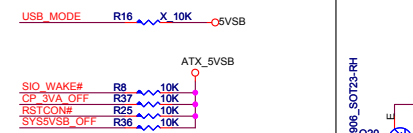
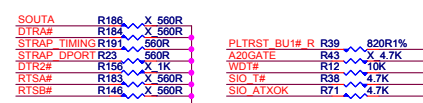
Sheet 23 of 41



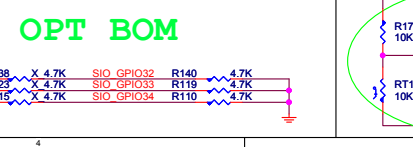
R15 10K USB MODE
 R11 100K H PECL
 USB MODE
 Hi By BIOS programming,
 default h/w PD for avoid UP7536 Enable pin floating

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP		Intel Cougar point
TIMING	AMD Timing	Timing
FANCTL	1/2/3	DAC Mode
STRAP		PWM Mode
DPORT (SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		

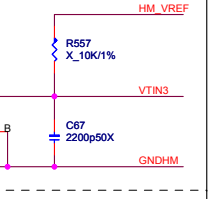


GPIO34 / GPIO33 / GPIO32	0	1	0
0	0	1	0
0	0	1	0
0	1	0	0



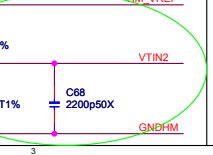
System Thermal

Close to Hot point S/IO

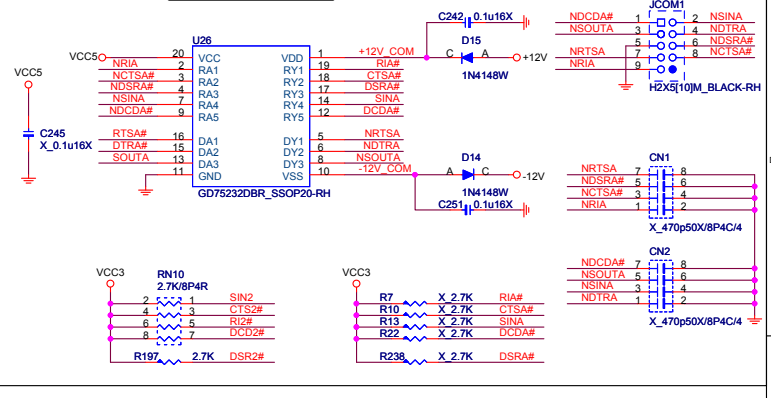


System Thermal

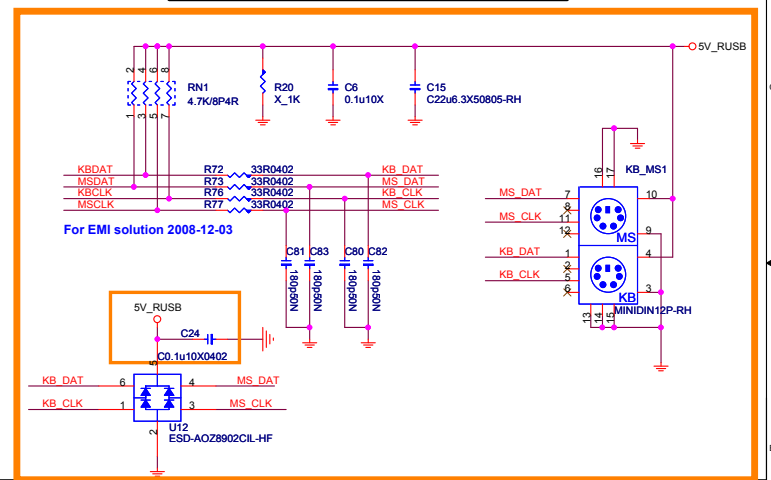
Close to Hot point MOS Q79



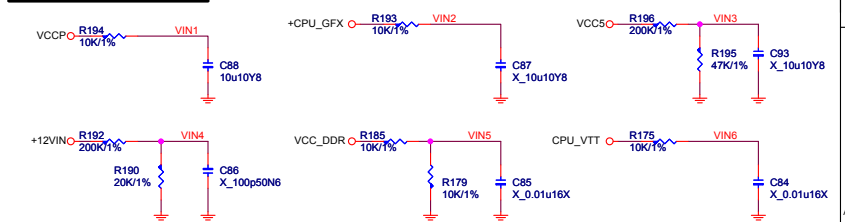
SERIAL PORT 1



PS2 KEYBOARD & MOUSE CONNECTOR



HW Monitor - Voltage



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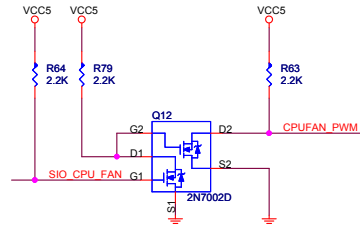
MS-7808

Size Custom Document Description
SIO-Fintek F71869AD

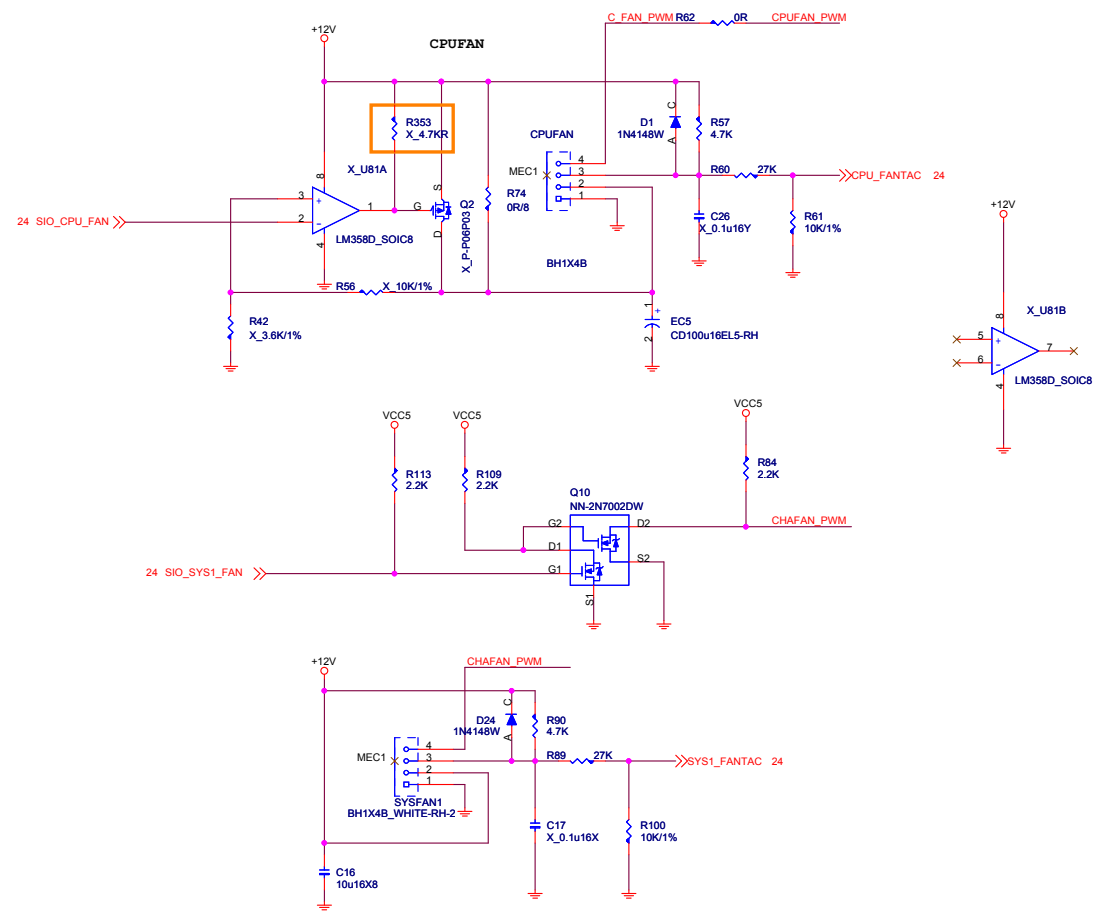
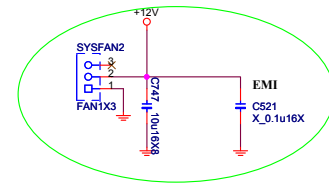
Rev 0A

Date: Monday, May 21, 2012 Sheet 24 of 41

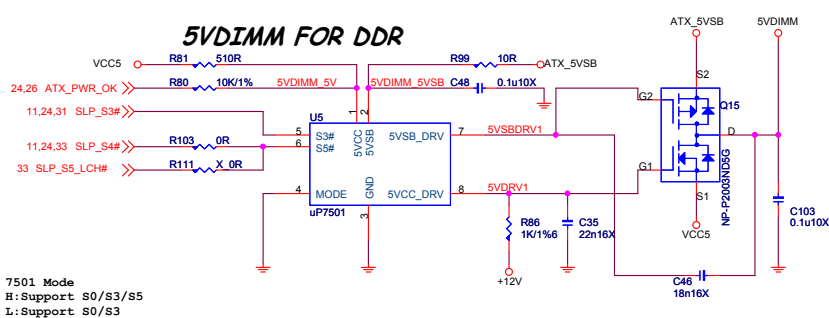
FAN-COUNTROL CIRCUIT



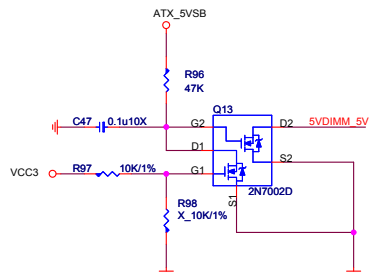
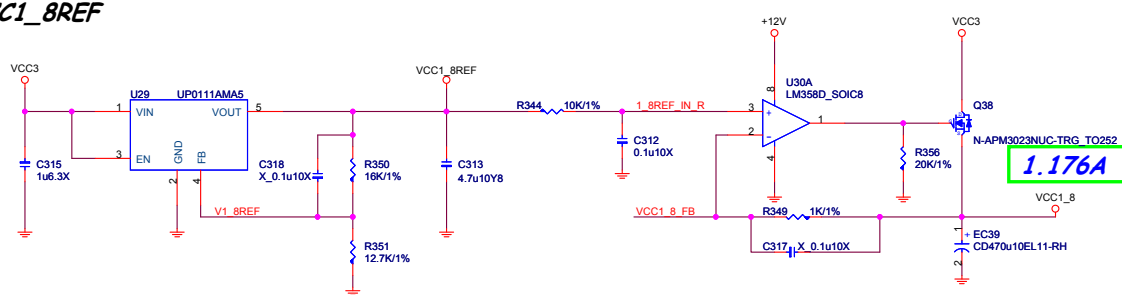
SYSTEM FAN1



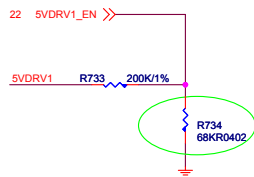
5VDIMM FOR DDR



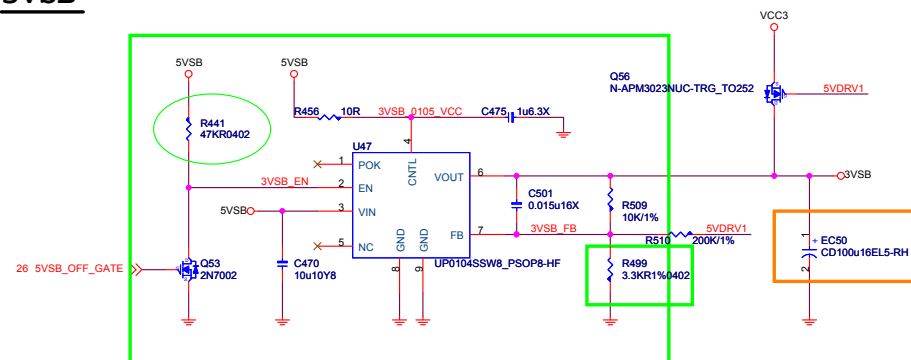
VCC1_8REF



USB MODE

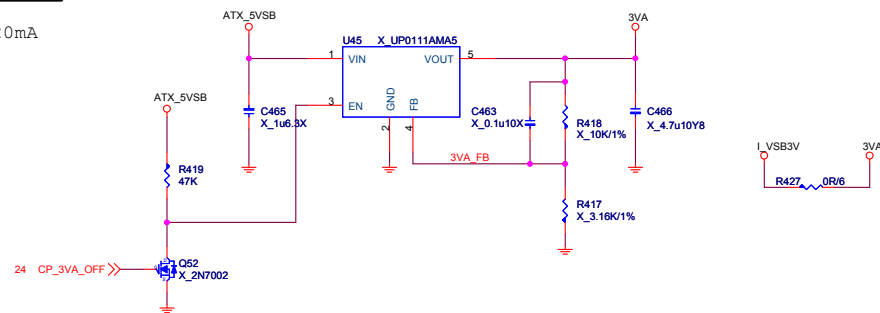


3VSB



3VA

20mA



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MS-7808

Size	Document Description	Rev
Custom	ACPI controller UPI	0A
Date: Friday, May 11, 2012	Sheet 27 of 41	

VRMPWRGD LEVEL SHIFT

CPU_VTT, 3VSB, VCC3, VRM_PGD_R, VR_HOT#, CPU_VTT, H_VIDSKL, H_VIDSOUT, CRB, SLP_S3_CTRL#

UPI VOLTAGE CONSOLE

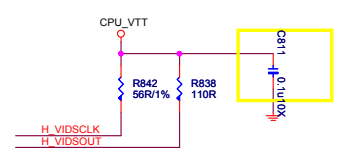
0x20 : RH=10K, RL=OPEN						
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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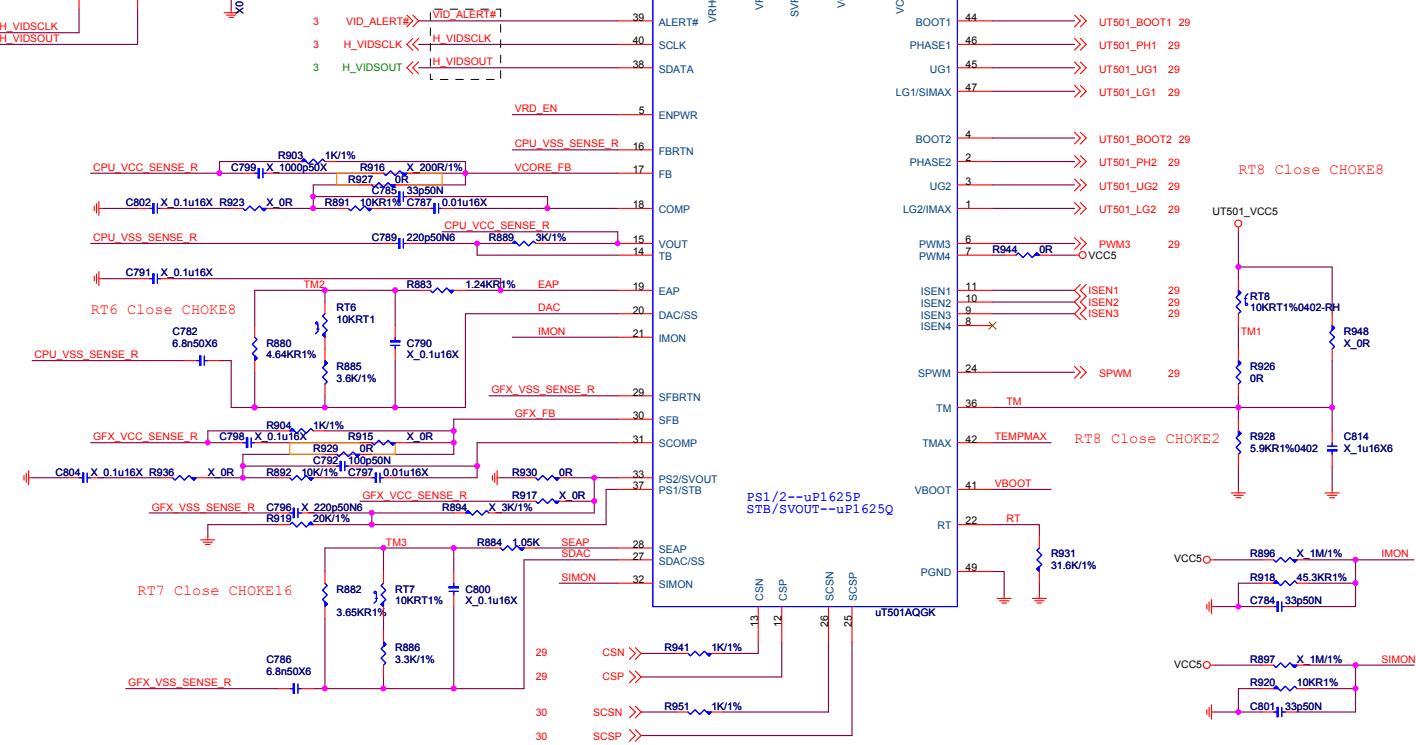
MS-7808

Size Custom Document Description **VRD12 - PWM-UT501** Rev 0A

Date: Tuesday, May 22, 2012 Sheet 28 of 41



3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



VRMPWRGD LEVEL SHIFT

CPU_VTT
3VSB
VCC3
VRM_PGD_R
VR_HOT#
VRD_EN
CPU_VCC_SENSE_R
CPU_VSS_SENSE_R
GFX_VCC_SENSE_R
GFX_VSS_SENSE_R
CSN
CSP
SCSP
SIMON
SEAP
SDAC/SS
PS1/SBOUT
PS1/SB
VBOOT
PGND
CHIP_PWGD

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

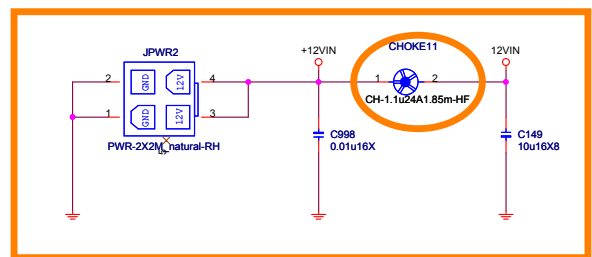
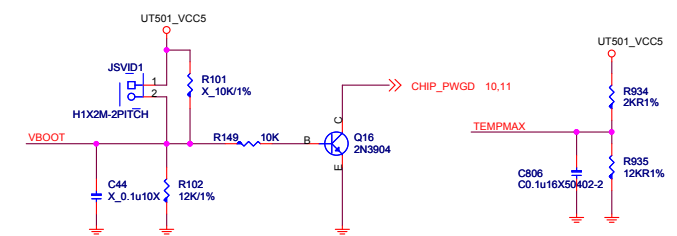
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MS-7808

Size Custom Document Description
VRD12 - PWM-UT501

Date: Tuesday, May 22, 2012 Sheet 28 of 41

0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

[illegible]

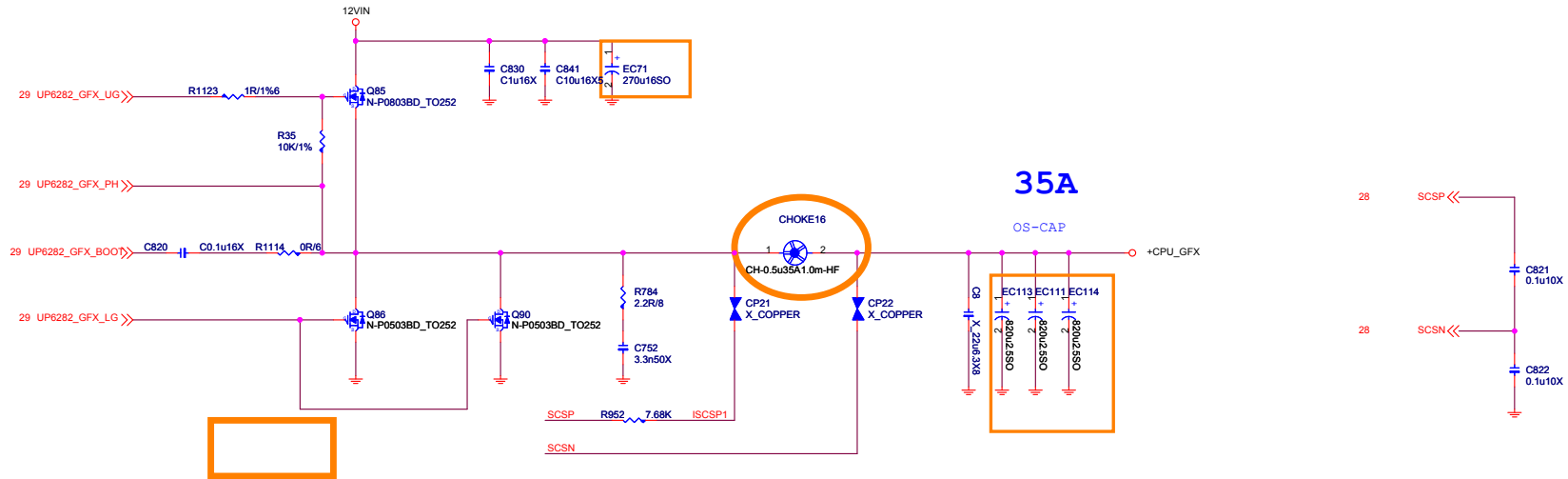
VRMPWRGD LEVEL SHIFT

CPU_VTT
3VSB
VCC3
VRM_PGD_R
VR_HOT#
VRM_PGD
CRB
SLP_S3_CTRL#
Q49 X_2N7002
CPU_VTT
H_VIDSKL
H_VIDSOUT
VID_ALERT#
H_VIDSKL
H_VIDSOUT
VID_ALERT#
VRD_EN
ENPWDR
FBRTN
FB
COMP
VOUT TB
EAP
DAC/SS
IMON
GFX_VSS_SENSE_R
GFX_FB
SFBRTN
SFB
SCOMP
PS2/SVOUT
PS1/STB
SEAP SDAC/SS
SIMON
CSN
CSP
SCSN
SCSP
UT501AQGK
VCC5
+12VIN
R878 2.2R/1%8
R879 2.2R/1%8
UT501 VCC12
C734 1u16X6
D29 Y Z
S-BAT54A_SOT23
UT501_BOOT1
UT501_BOOT2
VCC12
BOOT1
PHASE1
UG1
LG1/SIMAX
BOOT2
PHASE2
UG2
LG2/IMAX
PWM3
PWM4
ISEN1
ISEN2
ISEN3
ISEN4
SPWM
TM
TMAX
VBOOT
RT
PGND
UT501_VCC5
RT8 Close CHOKE8
RT8 Close CHOKE2
C814 X_1u16X6
VCC5
IMON
VCC5
SIMON
TEMPMAX
CHIP_PWGD 10,11
MSI
MICRO-STAR INT'L CO.,LTD
MS-7808
Size Custom
Document Description
VRD12 - PWM-UT501
Rev 0A
Date: Tuesday, May 22, 2012
Sheet 28 of 41

UPI VOLTAGE CONSOLE						
0x20 : RH=10K, RL=OPEN						
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

[illegible]

35A FOR CPU



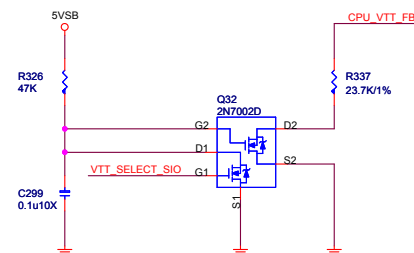
MICRO-STAR INT'L CO.,LTD

MS-7808

Size	Document Description
Custom	VRD12 -GPU 1-Phase MOS

Rev
0A

Date: Tuesday, May 22, 2012	Sheet 30 of 41
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$$5 \times 1 = 5A > 3.8A$$


CPU_SA:0.925/0.85

SA Core =8.8A

DDR Power:1.5V

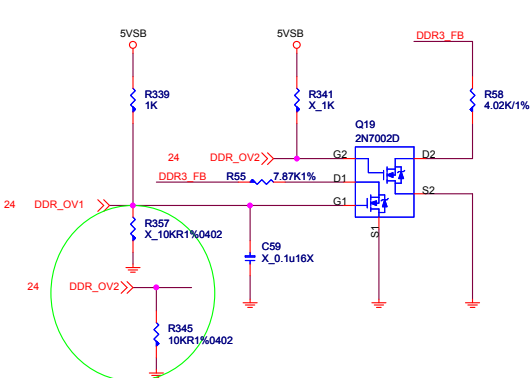
DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

5.5A FOR 2DIMM

0.5A FOR DDR VTT

DDR OV

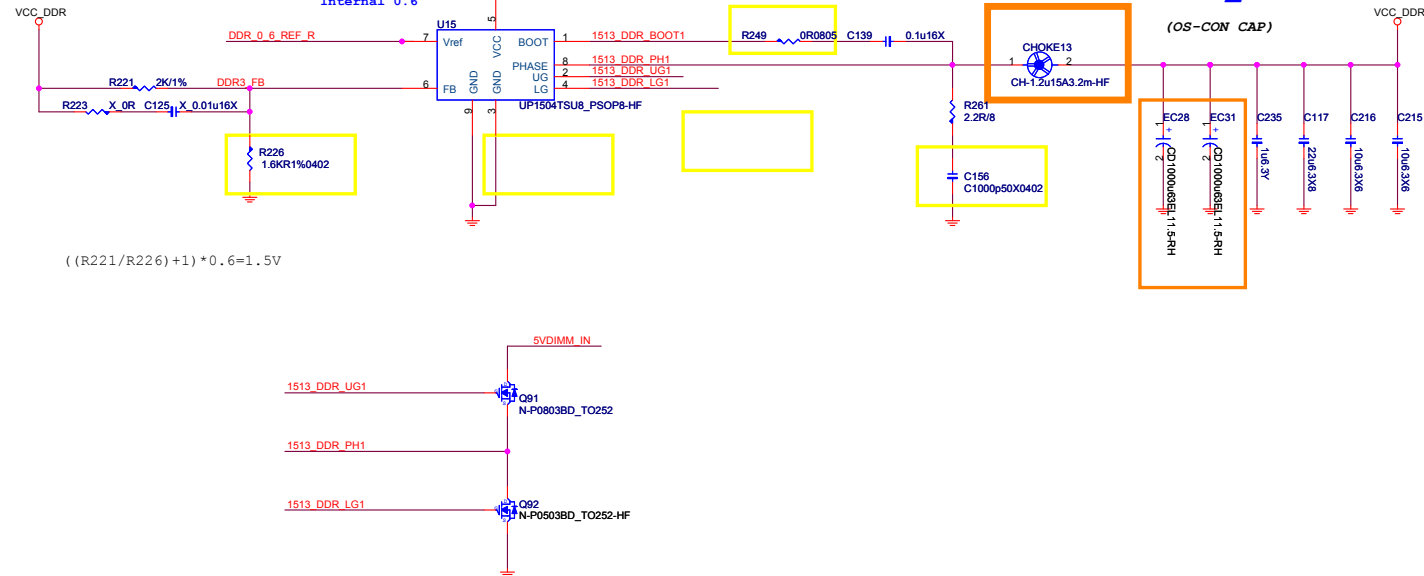


*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01 (S/IO)

DDR_OV2 = GPIO02 (S/IO)

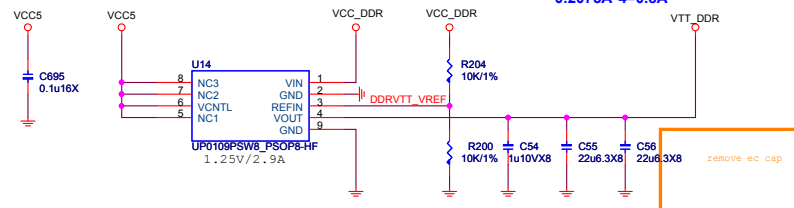


$$((R221/R226)+1)*0.6=1.5V$$

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$



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MS-7808

Size Custom	Document Description	Rev 0A
Date: Friday, May 18, 2012	DDR Power -UP1513 1-Phase MOS	
Sheet 33	of 41	

P.S. Only for meet Intel power down sequence.

PCH Power:1.05V

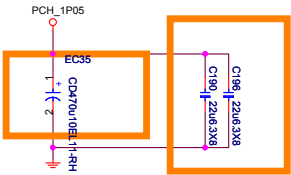
PCH Core 6.2A+0.105A+0.5A+0.08A=6.935A

6.2A FOR PCH

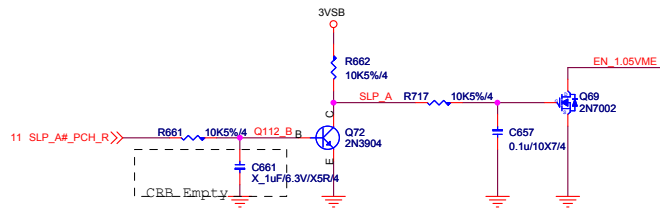
0.105A FOR VCCSSC

0.5A FOR VCCPLL

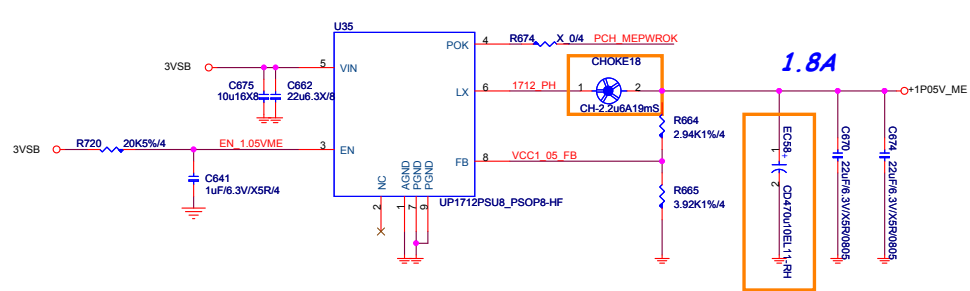
0.08A FOR VCCDMI



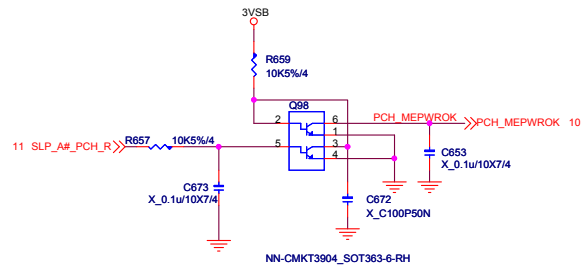
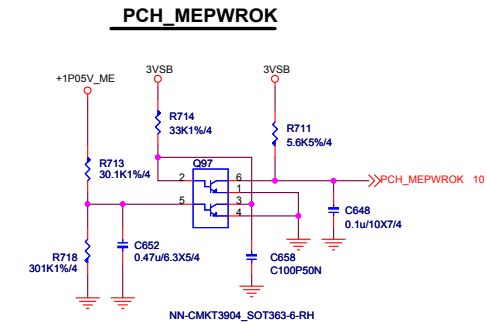
SLP_A



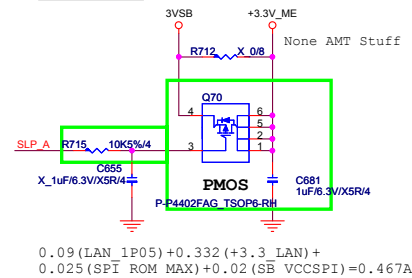
ME Power Control



+1.05V_ME(VCCIO_ME)



+3.3V_ME



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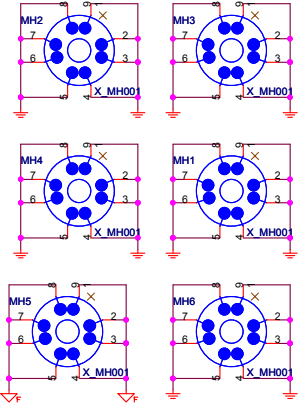
MS-7808

Size	Document Description	Rev
Custom	ME Power - UP1712	0A
Date: Friday, May 11, 2012	Sheet 35 of 41	

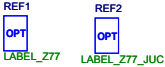
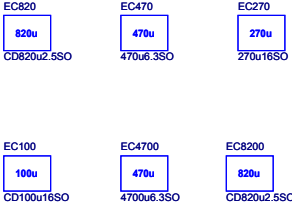
Mounting Holes



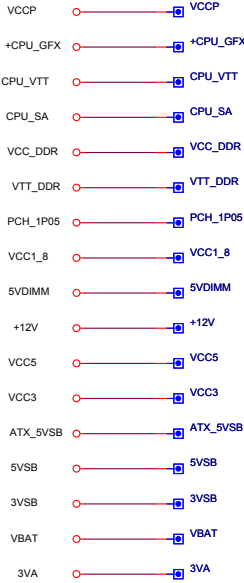
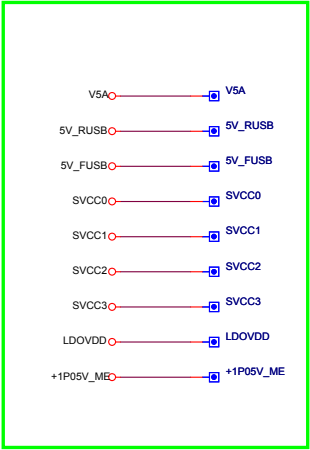
LA1
AMI_BIOS
LABEL
BIOS_LABEL



SOLID CAP



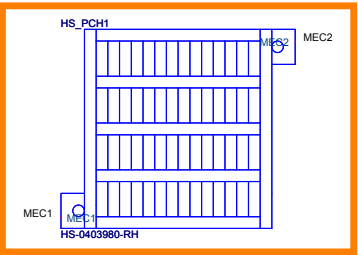
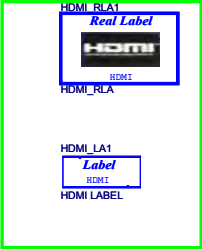
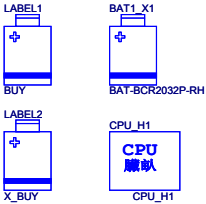
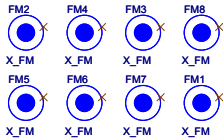
Voltage test point



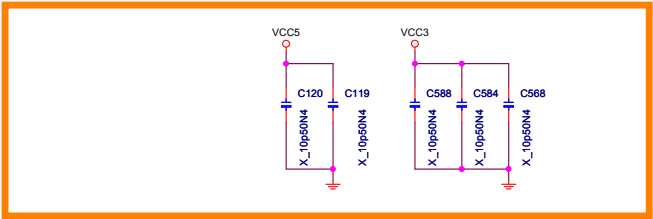
Simulation



Optical Fiducial Marks-120



EMI:cap. for signal return path



EMI

EMI

